REMARKS

Applicant has reviewed the comments, objections, and rejections set forth by the Examiner in the Office Action dated October 15, 2004 and respectfully respond with the amendments above and the following remarks. Claims 1-3, 6-12, and 17-21 are pending in the present case. Claims 1, 17, 19 and 20 are amended herein. Claims 14-16 are cancelled herein. Applicant respectfully requests reconsideration in view of the above amendments and the arguments set forth below.

ALLOWABLE SUBJECT MATTER

The Applicant respectfully thanks the Examiner for pointing out that Claims 1-3, 7-12, 17-19, and 20-21 contain allowable subject matter. Claims 14-16 are cancelled herein. Claim 17 is amended herein to incorporate the subject matter of Claims 14-16. Independent Claims 1 and 20 are amended herein to comport with 35 USC 112.

OBJECTIONS TO THE DRAWINGS

The drawings are objected to under 37 CFR 1.83(a), for an issue related to showing a ring oscillator. Applicant respectfully asserts that the ring oscillator is shown in a replacement drawing sheet for Figure 1, which was submitted with Applicant's response dated January 26, 2004, to the Office Action of September 26, 2003.

A duplicate copy of Applicant's January 26, 2004 response to that Office Action, including a duplicate copy of the replacement drawing sheet for Figure 1, is respectfully submitted herewith as Applicant's Exhibit 'A,' each page of which is stamped in blue ink with the word 'Duplicate.' Further, Applicant respectfully asserts that the subject ring oscillator is also shown in a replacement drawing sheet for Figure

1, which was submitted with Applicant's response dated August 6, 2003 to the Office Action of July 22, 2003. In Applicant's response dated August 6, 2003, the specification was amended to include the element number '150' for the subject ring oscillator. A duplicate copy of Applicant's August 6, 2003 response to that Office Action, including a duplicate copy of the replacement drawing sheet for Figure 1, is respectfully submitted herewith as Applicant's Exhibit 'B,' each page of which is stamped in blue ink with the word 'Duplicate.' Applicant respectfully asserts that the drawings comply with 37 CFR 1.121(d). Applicant respectfully requests the Examiner's review, withdrawal of objection, and approval.

CLAIM REJECTIONS

REJECTIONS UNDER 35 USC 112

Claims 1-3, 7-12, and 20-21 are rejected under 35 USC 112 (second paragraph). Claims 1 and 20 are amended herein to comport with the statute, in response to the Examiner's comments. As amended herein, Claims 1 and 20 read as follows, with underlining added for emphasis:

> 1. A circuit for controlling the rise time of a signal, comprising:
>
> a voltage multiplication circuit for converting an input voltage <u>corresponding to said signal</u> to an output voltage greater than said input voltage;
>
> a ramp generator coupled to said voltage multiplication circuit for controlling said output voltage from said voltage multiplication circuit, wherein a ratio between a first capacitor of said ramp generator and a second capacitor of said ramp generator determines said rise time of said signal, wherein said signal comprises a staircase ramp signal; and
>
> a divide by N counter coupled to said ramp generator for generating a plurality of clock phases wherein said ramp generator is controlled with said clock phases.

20. In a flash memory, a method for controlling a rise time of an on-chip generated voltage source used to program said flash memory, comprising:

generating a programming voltage VPP from a power supply, wherein said programming voltage is greater than a supply voltage VCC from said power supply;

activating a program control signal PGM to enable programming of a cell of said flash memory;

generating a stair-case ramp based on said programming voltage VPP in response to said program control signal PGM, wherein steps of said stair-case ramp have a period corresponding to a clock signal generated by a clock generator and voltage increases corresponding to a reference voltage times a ratio of two capacitor values.

As amended herein, independent Claims 1 and 20 have been corrected, and various signals recited therein have been clarified in accordance with the Examiner's comments. No new matter is added herein. Applicant respectfully asserts that Claims 1 and 20, as amended herein, recite subject matter as described in the specification, specifically from line 13 at page 5 through line 24 at page 11 (in the as-filed specification). (Applicant respectfully reminds the Examiner that the specification was amended in response to the Office Action of July 22, 2003, and respectfully refers the Examiner to that response, a duplicate copy of which is respectfully submitted herewith as Exhibit 'B,' discussed above.)

Applicant respectfully asserts that, as amended herein, independent Claims 1 and 20 and their respective dependent claims are definite. Thus, Applicant respectfully asserts that Claims 1-3, 7-12, and 20-21 are allowable under 35 USC 112 (second paragraph).

REJECTIONS UNDER 35 USC 102 AND OBJECTIONS TO CLAIMS

Claims 14-16 are rejected under 35 USC 102(b) over US Patent No. 5,539,351 to Gilsdorf, et al. (hereinafter Gilsdorf). (Applicant presumes from the reference numbers cited in the Office Action. The reference itself is apparently discussed without specific citation therein.) Applicant has reviewed the Gilsdorf reference and respectfully asserts that it does not anticipate the embodiments of the present invention as recited in Claims 14-16 for the following rationale.

Claims 14-16 are cancelled herein. Thus, Applicant respectfully asserts that their rejection under 35 USC 102(b) is moot.

Claims 17-19 are objected to as dependent upon rejected independent Claim 14. Applicant respectfully thanks the Examiner for pointing out that these Claims 17-19 "would be allowable if rewritten in independent form including all the limitations of the base claim and any intervening claims." Office Action of October 15, 2004 at page 4, last paragraph.

Claim 17 is amended herein. As amended herein, Claim 17 reads as follows:

> 17. A switched capacitor controller for controlling a rise time of an on-chip generated voltage source, comprising:
> a charge pump;
> a ramp generator coupled to said charge pump, wherein said ramp generator comprises a switched capacitor;
> a regulator circuit coupled to said switched capacitor circuit which causes a capacitor to switch between ground potential and the potential at a node, wherein a stair-step ramp signal is generated and said rise time is controlled with said switched capacitor,

wherein said switched capacitor controller performs a function related to programming a cell of said flash memory device, and wherein said switched capacitor comprises two capacitors wherein said rise time is controlled according to a ratio of capacitances of said two capacitors; and

an oscillator coupled to said charge pump which generates an oscillating signal to said charge pump.

As amended herein, Claim 17 recites, in independent form, all the limitations of the base Claim 14 and the intervening claims 15 and 16, which are all cancelled herein.

As Applicants understand the reference, Gilsdorf teaches a circuit and method for reducing a gate voltage of a transmission gate within a charge pump circuit. Gilsdorf at C.11/ll.50-63. However, Applicant finds no teaching or suggestion within the reference relating to either (1) performing a function related to the programming of flash memory cells, or (2) an oscillator coupled to a charge pump which generates an oscillating signal to the charge pump, as recited in Claim 17 herein. Thus, Applicant respectfully asserts that Gilsdorf does not anticipate Claims 17-19 herein.

Moreover, Applicant further understands Gilsdorf to teach that it is applicable to liquid crystal display (LCD) circuits. Id. at C.1/ll.44-50. In directing its teaching to LCD circuit applicability, Applicant respectfully asserts that the reference implicitly teaches away from the embodiments herein, which recite performing a function related to the programming of flash memory cells. Thus, Applicant respectfully asserts that the reference neither teaches nor suggests the embodiments recited herein.

While also not apparently discussed within the instant Office Action, US Patent No. 6,628,151 B1 to Zhou, et al. (hereinafter Zhou) is also cited. Applicant

has reviewed the Zhou reference and finds no teaching or suggestion therein relating to an oscillator coupled to a charge pump which generates an oscillating signal to the charge pump, as recited in Claim 17 herein. Thus, Applicant respectfully asserts that Zhou does not anticipate Claims 17-19 herein. Further, Applicant notes that the oscillator of Zhou's Figures 6 and 8 are not directly coupled to a charge pump, but are coupled to other elements. Thus Applicant respectfully asserts that Zhou implicitly teaches away from the embodiments recited herein, wherein the oscillator is coupled to a charge pump. Applicant respectfully asserts therefore that Zhou neither teaches nor suggests the embodiments recited in Claims 17-19 herein, and that these Claims 17-19 are allowable over the reference under 35 USC 102(b).

CONCLUSION

By the rationale stated above, the Applicant respectfully asserts that the drawings comply with 37 CFR 1.121(d), that Claims 1-3, 7-12 and 20-21 are allowable under 35 USC 112 (¶ 2), and that Claims 17-19 are allowable under 35 USC 102(b).

Accordingly, Applicants respectfully request that the objection to the drawings under 37 CFR 1.83(a), the rejection of Claims 1-3, 7-12 and 20-21 under 35 U.S.C. 112 (¶ 2), the rejection of Claims 14-16 under 35 U.S.C. 102(b) and the objections to Claims 17-19 be withdrawn and that Claims 1-3, 7-12, and 17-21 be allowed.

Please charge our deposit account No. 23-0085, for any unpaid fees.

Respectfully submitted,

WAGNER, MURABITO & HAO, LLP

Dated: Jan. 18, 2005

Lawrence B. Goerke
Reg. No. 45,927

WAGNER, MURABITO & HAO, LLP
Two North Market Street, Third Floor
San Jose, CA 95113

Tel.: (408) 938-9060
Fax: (408) 938-9069

U.S. Serial No. 10/015,033
CHUNG, Michael S.C., Inventor
Docket No. F0958

EXHIBIT 'A'

DUPLICATE

DUPLICATE

Amendment Transmittal

Applicant: **Chung** Filing Date: **12/11/01**

Docket No.: **AMD-F0958** Serial No.: **10/015,033**

Title: **A SWITCHED CAPACITOR CONTROLLER TO CONTROL THE RISE TIMES OF ON-CHIP GENERATED HIGH VOLTAGES**

Sir:

Please acknowledge receipt of the following:

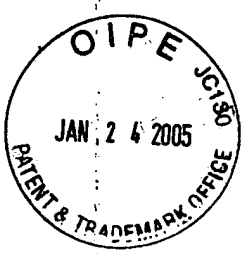
- Amendment (No. pgs 13)
- Amendment Transmittal
- Deposit Account Authorization
- Certificate of Mailing
- Copy of RCE packet filed 8/6/03
- Check # 0543 in the amount of **$110.00**

Submitted 1/26/04

COPY SENT 1/26/04 TO AMD

ENTERED 1-26-04

CDN



DUPLICATE

WAGNER, MURABITO AND HAO, LLP
GENERAL ACCOUNT
PH. (408) 938-9060
2 NORTH MARKET ST., 3RD FLOOR
SAN JOSE, CA 95113

CITIBANK
SAN JOSE, CA 95124
90-7118/3211 108

0543

PAY One Hundred Ten and No/100 Dollars

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COMMISSIONER FOR PATENTS

DUPLICATE

DATE 1/26/04

AMOUNT $110.00

Memo: AMD-F0958 1 MONTH EXT OF TIME

AUTHORIZED SIGNATURE

MP

⑈000543⑈ ⑆321171184⑆ 60165780⑈

Details on Back. Security Features Included

DUPLICATE

Attorney Docket No.: AMD-F0958

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

I hereby certify that this transmittal of the below described document is being deposited with the United States Postal Service in an envelope bearing First Class Postage and addressed to the Commissioner for Patents P.O. Box 1450, Alexandria, VA 22313-1450, on the below date of deposit.

Date of Deposit:	1/26/04	Name of Person Making the Deposit:	Kerry Erin Kelly	Signature of the Person Making the Deposit:	

OIPE JC1500 JAN 24 2005 PATENT & TRADEMARK OFFICE

In re Application of: **Chung**

Serial No.: **10/015,033** Examiner: **Nguyen, Hiep**

Filed: **12/11/01** Art Unit: **2816**

For: **A SWITCHED CAPACITOR CONTROLLER TO CONTROL THE RISE TIMES OF ON-CHIP GENERATED HIGH VOLTAGES**

Commissioner for Patents
Alexandria, VA 22313-1450

AMENDMENT TRANSMITTAL

1. Transmitted herewith is an amendment for this application

x Transmitted herewith is a response to an office action for the above identified patent application. (13 sheets)
____ Transmitted herewith are ____ Sheet of Proposed Drawing Amendments
____ Transmitted herewith is ____ sheet of drawings.
x Other: **Copy of RCE packet filed 8/6/03**

2. Applicant is other than a small entity

Extension of Term

3. The proceedings herein are for a patent application and the provisions of 37 C.F.R. 1.136 apply.

(a) [X] Applicant petitions for an extension of time under 37 C.F.R. 1.136 (fees: 37 C.F.R. 1.17(a)-(d) for the total number of months checked below:)

Extension	Fee
[X]one month	$ 110.00
[ ] two months	$ 420.00
[ ] three months	$ 950.00
[ ] four months	$1,480.00

Fee $

If an additional extension of time is required, please consider this a petition therefor.

(b) [ ] Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition for extension of time.

DUPLICATE

Fee Calculation

4. The fee for claims (37 C.F.R. 1.16(b)-(d)) has been calculated as shown below:

(for other than a small entity)					
Fee Items	Claims Remaining After Amendment	Highest Number of Claims Previously Paid For	Present Extra Claims	Fee Rate	Total
Total Claims	18	- 20 =	0	x $18.00	$0.00
Independent Claims	3	- 3 =	0	x $86.00	$0.00
Multiple Dependent Claim Fee (one or more, first added by this amendment)				$260.00	
Total Fees					**$00.00**

PAYMENT OF FEES

5. The full fee due in connection with this communication is provided as follows:

[x] The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No.: 23-0085. A duplicate copy of this authorization is enclosed.

[x] A check in the amount of $110.00

[ ] Charge any fees required or credit any overpayments associated with this filing to Deposit Account No.: 23-0085.

Please direct all correspondence concerning the above-identified application to the following address:

WAGNER, MURABITO & HAO LLP
Two North Market Street, Third Floor
San Jose, California 95113
(408) 938-9060

Respectfully submitted,

Date: January 26, 2004 By: _____

Lawrence R. Goerke
Reg. No. 45,927

DUPLICATE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

CHUNG, Michael S.C.

Serial No. 10/015,033

Filing Date: December 11, 2001

For: A SWITCHED CAPACITOR CONTROLLER TO CONTROL THE RISE TIMES OF ON-CHIP GENERATED HIGH VOLTAGES

Examiner: NGUYEN, Hiep

Group Art Unit: 2816

AMENDMENT AND RESPONSE TO OFFICE ACTION

Hon. Assistant Commissioner for Patents
P.O. Box No. 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office Action mailed on September 26, 2003, please amend the above captioned patent application as follows and consider the following remarks.

There are no amendments to the specification made in this responsive paper.

The Amendments to the Claims are reflected in the listing of the Claims, which begins on page 2 of this responsive paper.

The Remarks, with arguments, begin on page 6 of this responsive paper.

DUPLICATE

IN THE CLAIMS

Please amend the claims as shown below. This listing of claims will replace all prior versions and listings of claims in the Application.

1. (Currently Amended) A circuit for controlling the rise time of a signal, comprising:

a voltage multiplier which converts an input voltage to an output voltage greater than said input voltage;

a ramp generator coupled to said voltage multiplication circuit which controls said output voltage from said voltage multiplication circuit, wherein a ratio between a first capacitor of said ramp generator and a second capacitor of said ramp generator determines said rise time of said signal ; and

a divide by N counter coupled to said ramp generator.

2. (Original) The circuit of Claim 1, wherein said voltage multiplication circuit comprises a charge pump.

3. (Original) The circuit of Claim 1, wherein said signal is used to program and erase Flash EPROM cells.

4. (Cancelled)

5. (Original) The circuit of Claim 1, wherein said signal comprises a staircase ramp signal.

6. (Canceled)

DUPLICATE

7. (Previously Amended) The circuit of Claim 1 further comprising a level shifter.

8. (Original) The circuit of Claim 1 further comprising two non-overlapping clock signals.

9. (Previously Amended) The circuit of Claim 1 further comprising a ring oscillator coupled to said ramp generator.

10. (Previously Amended) The circuit of Claim 1 further comprising a capacitor divider network coupled to a switched capacitor network.

11. (Currently Amended) The circuit of Claim 10, wherein said switched capacitor network switches between ground potential and potential of a node of said capacitor divider network.

12. (Previously Amended) The circuit of Claim 11, wherein said node is coupled to a CMOS comparator.

13. (Cancelled)

14. (Currently Amended) A switched capacitor controller for controlling a rise time of an on-chip generated voltage source, comprising:

a charge pump;

a ramp generator coupled to said charge pump, wherein said ramp generator comprises a switched capacitor ;

DUPLICATE

a regulator circuit coupled to said switched capacitor circuit which causes a capacitor to switch between ground potential and the potential of a node, wherein a stair-step ramp signal is generated and said rise time is controlled according to said switched capacitor.

15. (Original) The switched capacitor controller of Claim 14, wherein said rise time is controlled according to a ratio of two capacitors.

16. (Original) The switched capacitor controller of Claim 14, wherein said on-chip generated voltage source is used to program a Flash memory.

17. (Original) The switched capacitor controller of Claim 14 further comprising an oscillator coupled to said charge pump which generates an oscillating signal to said charge pump.

18. (Original) The switched capacitor controller of Claim 17 further comprising:

a divider coupled to said oscillator;

a non-overlapping two phase clock generator coupled to said divider.

19. (Original) The switched capacitor controller of Claim 14, wherein said ramp generator further comprises a capacitor divider network.

20. (Currently Amended) In a flash memory, a method for controlling a rise time of an on-chip generated voltage source used to program said flash memory, comprising:

generating a programming voltage VPP from a power supply, wherein said programming voltage is greater than voltage VCC from said power supply;

activating a program signal to program a cell of said flash memory;

generating a stair-case ramp based on said programming voltage in response to said program signal, wherein steps of said stair-case ramp have a period corresponding to a clock signal generated by a clock generator and voltage increases corresponding to a reference voltage times a ratio of two capacitor values.

21. (Currently Amended) The method of Claim 20 further comprising ~~the step of~~ switching a capacitor between ground potential and the potential of a node voltage to generate said stair-case ramp.

DUPLICATE

REMARKS

Claims 1-3, 5, 7-12, and 14-21 are pending in the present case. Claims 4 and 6 were cancelled previously; Claim 13 is cancelled herein. Claims 1, 11, 14, 20, and 21 are amended herein. Applicants respectfully request reconsideration in view of the above amendments to the present application, and the arguments set forth below. No new matter is added herein.

ALLOWABLE SUBJECT MATTER

The Applicant respectfully thank the Examiner for pointing out that Claims 11-13 contained allowable subject matter. Claim 13 is cancelled herein. Claim 1 is amended herein to incorporate the allowable subject matter of Claim 13.

OBJECTIONS TO THE DRAWINGS

The drawings are objected to under 37 CFR 1.83(a) for not depicting the oscillators recited in Claims 9, 17, and 18. The Applicant respectfully point out that a corrected Replacement Sheet for Figure 1 was provided with the Request for Continuing Examination (RCE) filed by the Applicant on August 6, 2003, wherein this Replacement Sheet depicts the oscillator element labeled by marker label --150--. Further, the RCE filed August 6, 2003 amended the specification to effect this change to Figure 1. A duplicate of this Replacement Sheet, along with a copy of the original sheet provided for Figure 1, is attached hereto, along with a copy of the RCE of August 6, 2003. The Applicant respectfully requests the Examiner's review and approval.

DUPLICATE

REJECTIONS OF THE CLAIMS UNDER 35 USC 112

In the Office Action, Claims 14-21are rejected as indefinite under 35 USC 112 (second paragraph). Claim 14 was rejected as misdescriptive for reciting "which causes a capacitor to switch between ground and a node". As amended herein, Claim 14 reads as follows:

> 14. (Currently Amended) A switched capacitor controller for controlling a rise time of an on-chip generated voltage source, comprising:
> a charge pump;
> a ramp generator coupled to said charge pump, wherein said ramp generator comprises a switched capacitor;
> a regulator circuit coupled to said switched capacitor circuit which causes a capacitor to switch between ground potential and the potential of a node, wherein a stair-step ramp signal is generated and said rise time is controlled according to said switched capacitor.

(underlining added herein for emphasis). As amended herein, Claim 14 recites that the capacitor is caused to switch between ground potential and the potential of a node. The Applicant respectfully asserts that, by delineating the potentials between which the capacitor is switched, Claim 14, as amended herein, is definite under 35 USC 112 (second paragraph).

Claim 20 was rejected as indefinite because the clock signal recited in the claim was not clear from the drawings. As amended herein, Claim 20 reads as follows:

DUPLICATE

20. (Currently Amended) In a flash memory, a method for controlling a rise time of an on-chip generated voltage source used to program said flash memory, comprising:

generating a programming voltage VPP from a power supply, wherein said programming voltage is greater than voltage VCC from said power supply;

activating a program signal to program a cell of said flash memory;

generating a stair-case ramp based on said programming voltage in response to said program signal, wherein steps of said stair-case ramp have a period corresponding to a clock signal <u>generated by a clock generator</u> and voltage increases corresponding to a reference voltage times a ratio of two capacitor values.

(underlining added herein for emphasis). As amended herein, Claim 14 recites that the clock signal is generated by a clock generator, such as that depicted by element number 103 of Figure 1. The Applicant respectfully asserts that, by delineating that the clock signal is generated by a clock generator depicted in the drawing figures, Claim 20, as amended herein, is definite under 35 USC 112 (second paragraph).

In the Office Action, Claims 15-19 and 21 were also rejected under 35 USC 112 (second paragraph) as indefinite, due to the technical deficiencies of Claims 1 (sic) and 20. The Applicant respectfully assumes that the Examiner meant that Claims 15-19 were rejected due to technical deficiencies of Claim <u>14</u>. Claims 15-19 depend upon independent Claim 14, and thus incorporate each and every one of its elements. As above, Applicant respectfully asserts that Claim 14, as amended herein, is sufficiently definite under 35 USC 112 (second paragraph). Thus, Applicant respectfully asserts that its dependent Claims 15-19 are sufficiently definite as well.

DUPLICATE

Likewise, Claim 20 depends upon independent Claim 20, and thus incorporate each and every one of its elements. As above, Applicant respectfully asserts that Claim 20, as amended herein, is sufficiently definite under 35 USC 112 (second paragraph). Thus, Applicant respectfully asserts that its dependent Claim 21 is sufficiently definite as well.

The Applicant respectfully asserts that, as amended herein, Claims 14-19 and 20-21 are definite under 35 USC 112 (second paragraph). Applicant respectfully requests the Examiner's review and allowance.

REJECTIONS OF THE CLAIMS UNDER 35 USC 102

Claims 1-3, 5, and 7-10 are rejected under 35 USC 102(b) as anticipated by US Patent No. 5,168,174 to Naso, et al., hereinafter the Naso reference. Applicants have reviewed the reference cited and respectfully assert it does not anticipate the embodiments of the present invention as recited in Claims 1-3, 5, and 7-10 for the following rationale.

As Applicants understand the reference, Butts teaches a negative voltage charge pump with feedback control. However, Butts does not teach or suggest a circuit having either:

(1) a divide by N counter coupled to a ramp generator,

(2) a switched capacitor network switches between ground potential and the potential of a node of a capacitor divider network, or

(3) a node is coupled to a CMOS comparator,

all of which are pointed out as allowable subject matter by the Examiner. Thus, Butts differs from the embodiment of the present invention recited by Claim 1, as amended herein.

DUPLICATE

As amended herein, Claim 1 reads as follows:

1. (Currently Amended) A circuit for controlling the rise time of a signal, comprising:

a voltage multiplier which converts an input voltage to an output voltage greater than said input voltage;

a ramp generator coupled to said voltage multiplication circuit which controls said output voltage from said voltage multiplication circuit, wherein a ratio between a first capacitor of said ramp generator and a second capacitor of said ramp generator determines said rise time of said signal ; and

a divide by N counter coupled to said ramp generator.

(underlining added herein for emphasis). Claim 13 is cancelled herein. The allowable subject matter of Claim 13, relating to a divide-by-N counter, has been incorporated into Claim 1, as amended herein, such that Claim 1, as amended herein, recites the divide-by-N counter.

A divide-by-N counter is not taught of suggested by Naso. Thus, the Applicant respectfully asserts that Naso does not anticipate or suggest the embodiment of the present invention recited by Claim 1, as amended herein. The Applicant thus respectfully asserts that Claim 1, as amended herein, overcomes Naso. Applicant respectfully asserts therefore that Claim 1, as amended herein, and its dependent Claims 2-3, 5, and 7-12 are allowable under 35 USC 102(b). The Applicant respectfully requests the Examiner's review and allowance.

CONCLUSION

By the rationale stated above, the Applicant respectfully asserts that the embodiments of the present invention as recited in Claims14-21 are definite under 35 USC 112 (second paragraph). Further, by the rationale stated above, the

Applicant respectfully asserts that the embodiments of the present invention as recited in Claims 1-3, 5, and 7-12 are allowable under 35 USC 102(b). The Applicant respectfully asserts therefore that Claims 1-3, 5, 7-12, and 14-21 are in condition for allowance. Accordingly, Applicants respectfully request that the rejection of Claims 14-21 under 35 U.S.C. 112 (second paragraph) and of Claims 1-3, 5, and 7-10 under 35 U.S.C. 102(b) be withdrawn and that Claims 1-3, 5, 7-12, and 14-21 be timely allowed.

Please charge our deposit account No. 23-0085, for any unpaid fees.

Respectfully submitted,

WAGNER, MURABITO & HAO, LLP

Dated: Jan. 26, 2004

Lawrence R. Gaerke
Registration No. 45,927

WAGNER, MURABITO & HAO, LLP
Two North Market Street, Third Floor
San Jose, CA 95113

Tel.: (408) 938-9060
Fax: (408) 938-9069

DUPLICATE

Replacement Sheet

DUPLICATE

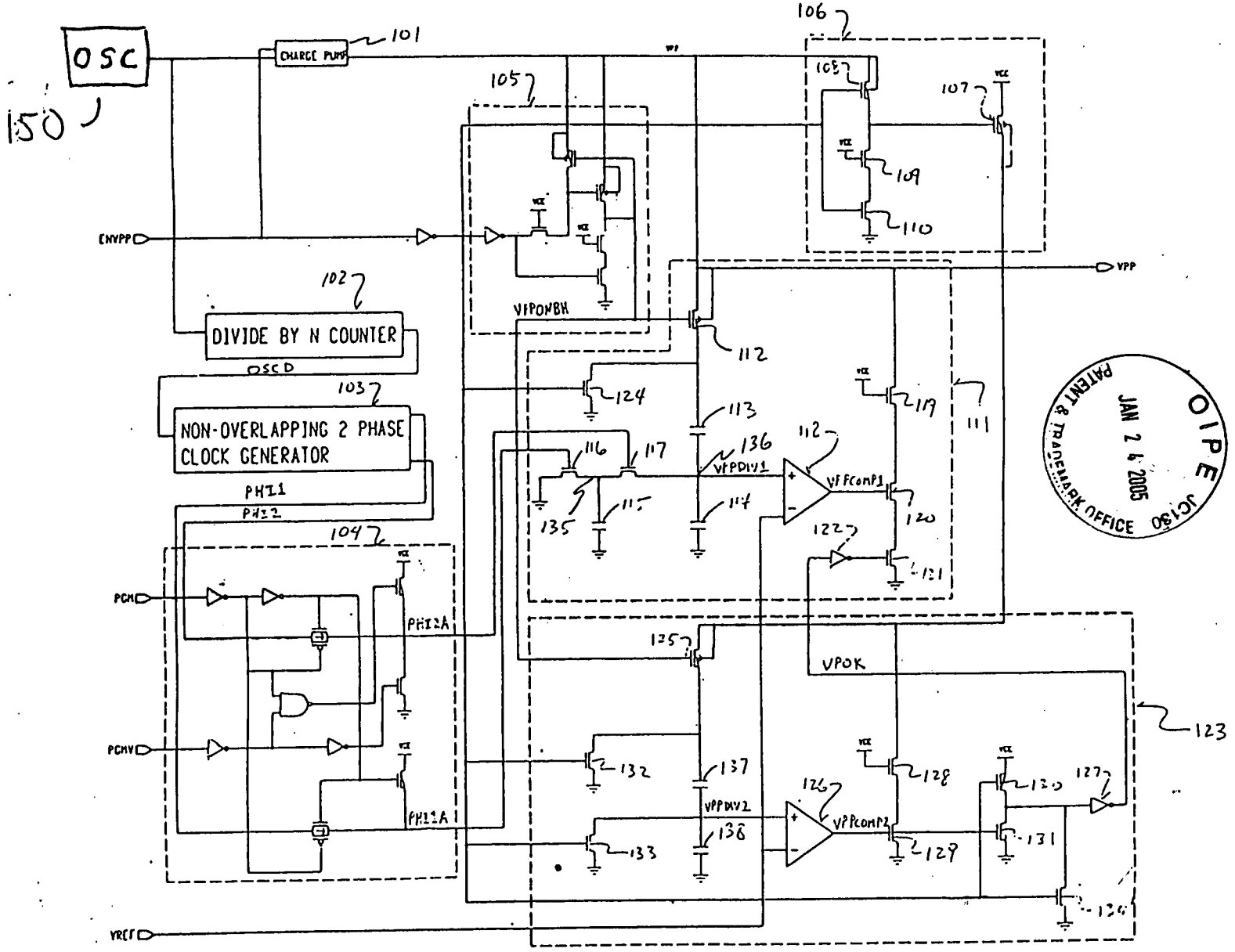

Figure 1

DUPLICATE

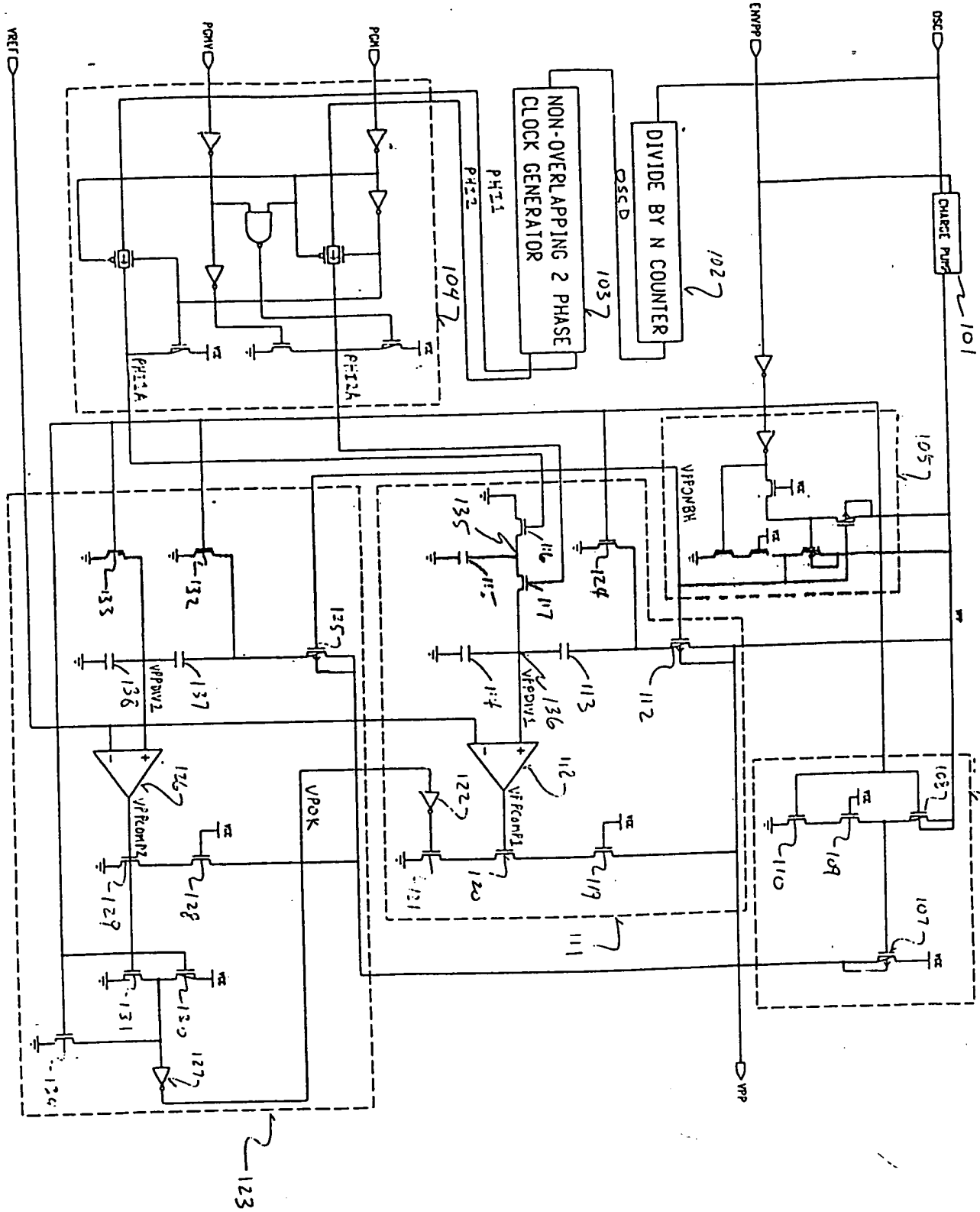

Figure 1

U.S. Serial No. 10/015,033
CHUNG, Michael S.C., Inventor
Docket No. F0958

EXHIBIT 'B'

DUPLICATE

DUPLICATE

RCE Transmittal

Applicant: **Michael S.C. Chung** Filing Date: **12/11/01**

Docket No.: **AMD-F0958** Serial No.: **10/015,033**

Title: **A SWITCHED-CAPACITOR CONTROLLER TO CONTROL THE RISE TIMES OF ON-CHIP GENERATED HIGH VOLTAGES**

DUPLICATE

Sir: Please acknowledge receipt of the following:

- Preliminary Amendment 11 Sheets
- RCE Transmittal
- Replacement Drawings (1 sheet)
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- Express Mail Certificate **EV302956450US**

ENTERED 8-6-03

CDB

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WAGNER, MURABITO & HAO LLP
COST ADVANCED CREDIT LINE
2 NORTH MARKET ST., 3rd FLOOR 408-938-9060
SAN JOSE, CA 95113

Citibank (West), FSB
90-7118/3211

13716

DUPLICATE

Eight Hundred Sixty and No/100 Dollars

DATE
8/6/03

AMOUNT
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THE
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ASSISTANT COMMISSIONER FOR PATENTS

WAGNER, MURABITO & HAO LLP

AUTHORIZED SIGNATURE

Memo: AMD-F0958 FILING FEE-RCE

⑈013716⑈ ⑆321171184⑆ 20007045 6⑈

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Patent Application

I hereby certify that this transmittal of the below described documents is being deposited with the United States Postal Service in an envelope bearing Express Mail Postage and an Express Mail label, with the below serial number, addressed to Mail Stop RCE, Commissioner For Patents, Alexandria, VA 22313-1450 on the below date of deposit.			
Express Mail Label No.:	EV302956450US	Name of Person Making the Deposit:	ANTHONY CHOU
Date of Deposit:	8/06/03	Signature of the Person Making the Deposit:	Anthony Chou

In re Application of: **CHUNG, Michael S.C.**

Serial No.: **10/015,033** Examiner: **NGUYEN, H.**

Filed: **12/11/01** Art Unit: **2816**

For: **A SWITCHED-CAPACITOR CONTROLLER TO CONTROL THE RISE TIMES OF ON-CHIP GENERATED HIGH VOLTAGES**

Mail Stop RCE
Commissioner For Patents
Alexandria, VA 22313-1450

DUPLICATE

REQUEST FOR CONTINUED EXAMINATION (RCE) TRANSMITTAL
(SUBSECTION(B) OF 35 U.S.C. § 132)

This is a Request for Continued Examination (RCE) under 37 C.F.R. § 1.114 for the above-identified application.

1. Submission required under a filing under 37 C.F.R. § 1.114

   a. [ ] Previously submitted

   i. [ ] Consider the amendment(s)/ reply under 37 C.F.R. § 1.116 previously filed on _____
   (Any unentered amendment(s) referred to above will be entered)

   ii. [ ] Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____

   iii. [ ] Other _____

   b. [**X**] Enclosed

   i. [**X**] Amendment/Reply

   DUPLICATE

   ii. [ ] Affidavit(s)/Declaration(s)

   iii. [ ] Information Disclosure Statement (IDS)

   iv. [**X**] Other 1 sheet of replacement drawings

2. Miscellaneous

   a. [ ] Suspension of action on the above-identified application is requested under 37 C.F.R. § 1.103(c) for a period of _____ months.
   (period of suspension shall not exceed 3 months: Fee under 37 C.F.R. § 1.17(l) required)

   b. Other _____

DUPLICATE

Extension of Term

3. The proceedings herein are for a patent application and the provisions of 37 C.F.R. 1.136 apply.

(a) [X] Applicant petitions for an extension of time under 37 C.F.R. 1.136 (fees: 37 C.F.R. 1.17(a)-(d) for the total number of months checked below:)

Extension	Fee
[X] one month	$110.00
[ ] two months	$400.00
[ ] three months	$920.00
[ ] four months	$1,440.00

Fee $110.00

If an additional extension of time is required, please consider this a petition therefor.

(b) [ ] Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition for extension of time.

FEES DUE

The RCE fee under 37 C.F.R. § 1.17(e) is required by 37 C.F.R. § 1.114 when the RCE is filed.

CLAIMS					
	NO. OF CLAIMS		EXTRA CLAIMS	RATE	FEES
Basic Application Fee					$750.00
Total Claims	21	Minus Highest Prev. Paid	0	X $18 =	$0.00
Independent Claims	3	Minus Highest Prev. Paid	0	X $84 =	$0.00
If multiple dependent claims are presented, add $260.00					$0.00
TOTAL APPLICATION FEE DUE					**$750.00**

PAYMENT OF FEES

1. The full fee due in connection with this communication is provided as follows:

[X] The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No.: 23-0085. A duplicate copy of this authorization is enclosed.

[X] A check in the amount of $ 860.00

DUPLICATE

DUPLICATE

[ ] Charge any fees required or credit any overpayments associated with this filing to Deposit Account No.: 23-0085.

Please direct all correspondence concerning the above-identified application to the following address:

WAGNER, MURABITO & HAO LLP
Two North Market Street, Third Floor
San Jose, California 95113
(408) 938-9060

Respectfully submitted,

Date: August 6, 2003

By: _____
Mehlin Dean Matthews
Reg. No. 46,127

DUPLICATE

DUPLICATE

PAMD-F0958

DUPLICATE

Patent

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of :	)	
	)	
Chung, Michael S.C.	)	Examiner: Nguyen, H.
	)	
Serial No.: 10/015,033	)	Art Unit: 2816
	)	
Filed: 12/11/01`	)	
	)	
For: A SWITCHED-CAPACITOR CONTROLLER TO CONTROL THE RISE TIMES OF ON-CHIP GENERATED HIGH VOLTAGES	)	

AMENDMENT AND RESPONSE TO OFFICE ACTION

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Office Action mailed July 22, 2003 for the above captioned patent application, Applicant respectfully requests entry of the following amendments and consideration of the following remarks.

DUPLICATE

AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph on page 5 beginning with "Referring to Figure 1..." with the following paragraph:

Referring to Figure 1, a circuit diagram of the currently preferred embodiment of the present invention is shown. The circuit comprises a charge pump 101. Alternatively, a voltage multiplication circuit may be implemented in place of the charge pump 101. The charge pump 101 is typically comprised of a series of MOS diode connected transistors and coupling capacitors driven by two-phase non-overlapping clocks generated from a primary clock signal ~~labeled~~ OSC. The OSC signal is usually the output of an on-chip ring oscillator circuit 150. The OSC signal is also input to the divide by N counter 102. The divide by N counter 102 is a binary digital counter that performs a "divide by N" function where N is a power of two. The output from the divide by N counter 102 is a clock signal, OSCD, whose frequency is equal to that OSC divided by N where $N=2^M$, with being the width ~~of~~ in bits of the binary counter represented by the counter. The OSCD output from the divide by N counter 102 is fed as an input to the non-overlapping two-phase clock generator 103. The clock generator 103 generates two non-overlapping clock phases, PHI1 and PHI2, which have the same frequency as the output from the counter 102. The two non-overlapping clock phase signals are input to block 104. Block 104 creates two "gated" versions of the PHI1 and PHI2 signals, referred to as PHI1A and PHI2A. The PHI1A and PHI2A signals are controlled by the control signals PGM and PGMV. When both PGM and PGMV are low, both PHI1A and PHI2A are pulled up to logic high (e.g., V_{CC}). When PGMV is high and PGM is low, PHI1A is

pulled up to V_{CC} while PHI2A is grounded. Finally, when PGMV is low and PGM is high, PHI1A is logically equivalent to PHI1 while PHI2A is equivalent to PHI2. In other words, when PGM is high and PGMV is low, PHI1A and PHI2A function as a pair of non-overlapping two phase clock signals. It should be noted that, by design, there will never be a situation whereby both PGM and PGMV are both high. Circuit block 105 comprises a voltage level shifter that converts the control signal ENVPP to a level shifted inverted signal, VPPONBH.

AMENDMENTS TO THE DRAWINGS

An amended Figure 1 is attached. The amendment to Figure 1 is described in the Remarks. No new matter has been added.

LISTING OF THE CLAIMS (1-21) DUPLICATE

Claim 1 (currently amended): A circuit for controlling a rise-time of a signal, comprising:

a voltage multiplication circuit which converts an input voltage to an output voltage greater than said input voltage;

a ~~switched capacitor circuit~~ ramp generator coupled to said voltage multiplication circuit which controls said output voltage from said voltage multiplication circuit, wherein a ratio between a first capacitor of said ramp generator ~~switched capacitor circuit~~ and a second capacitor of said ramp generator ~~switched capacitor circuit~~ determines said rise-time of said signal~~, said circuit for controlling a rise time of a signal further comprises a constant ramp generator~~.

Claim 2 (original): The circuit of Claim 1, wherein said voltage multiplication circuit comprises a charge pump.

Claim 3 (original): The circuit of Claim 1, wherein said signal is used to program and erase Flash EPROM cells.

Claim 4 (canceled)

Claim 5 (original): The circuit of Claim 1, wherein said signal comprises a staircase ramp signal.

DUPLICATE

Claim 6 (canceled) DUPLICATE

Claim 7 (currently amended): The circuit of Claim 1 further comprising a level shifter ~~to shut off said signal~~.

Claim 8 (original): The circuit of Claim 1 further comprising two non-overlapping clock signals.

Claim 9 (currently amended): The circuit of Claim 1 further comprising a ring oscillator coupled to said ramp generator ~~switched capacitor circuit~~.

Claim 10 (currently amended): The circuit of Claim 1 further comprising a capacitor divider network coupled to ~~said~~a switched capacitor ~~circuit~~network.

Claim 11 (currently amended): The circuit of Claim 10, wherein said switched capacitor ~~circuit~~ network switches between ground and a node of said capacitor divider network~~divider node which has a constant reference voltage according to a feed back system~~.

Claim 12 (currently amended): The circuit of Claim 11, wherein said node is coupled to~~feedback system comprises~~ a CMOS comparator.

Claim 13 (original): The circuit of Claim 1 further comprising a divide by N counter.

Claim 14 (previously amended): A switched capacitor controller for controlling a rise time of an on-chip generated voltage source, comprising:

a charge pump;

a ramp generator coupled to said charge pump, wherein said ramp generator comprises a switched capacitor;

a regulator circuit coupled to said switched capacitor circuit which causes a capacitor to switch between ground and a node, wherein a stair-step ramp signal is generated and said rise time is controlled according to said switched capacitor.

Claim 15 (original): The switched capacitor controller of Claim 14, wherein said rise time is controlled according to a ratio of two capacitors.

Claim 16 (original): The switched capacitor controller of Claim 14, wherein said on-chip generated voltage source is used to program a Flash memory.

Claim 17 (original): The switched capacitor controller of Claim 14 further comprising an oscillator coupled to said charge pump which generates an oscillating signal input to said charge pump.

Claim 18 (original): The switched capacitor controller of Claim 17 further comprising:

a divider coupled to said oscillator;

a non-overlapping two phase clock generator coupled to said divider.

DUPLICATE

Claim 19 (original): The switched capacitor controller of Claim 14, wherein said ramp generator further comprises a capacitor divider network.

Claim 20 (currently amended): In a flash memory, a method for controlling a rise time of an on-chip generated voltage source used to program said flash memory, comprising:

generating a programming voltage VPP from a power supply, wherein said programming voltage is greater than voltage VCC from said power supply;

activating a program signal to program a cell of said flash memory;

generating a stair-case ramp based on said programming voltage in response to said program signal, wherein steps of said stair-case ramp have a period corresponding to a clock signal and voltage increases corresponding to a reference voltage times a ratio of two capacitor values.

Claim 21 (original): The method of Claim 20 further comprising the step of switching a capacitor between ground and a node voltage to generate said staircase ramp.

DUPLICATE

REMARKS

The objections, rejections and comments of the Examiner set forth in the Office Action dated April 7, 2003 have been carefully reviewed by the Applicant.

The drawing are objected to under 37 CFR 1.83(a) for failing to show every feature of the invention specified in the claims. With respect to a "ring oscillator" and "oscillator," Figure 1 has been amended to include a box labeled "150" around the signal terminal "OSC" to represent an oscillator that is the source of the signal "OSC." In addition, the specification has been amended to attribute the label "150" to the ring oscillator described as the source of the signal "OSC" in the specification at page 5, lines 19-20.

With respect to a "regulator circuit," the Applicant points out that the regulator circuit is shown in Figure 1 (in block 123), and described in the specification at page 8, lines 10-17.

With respect to "a programming voltage," the Applicant points out that the voltage VPP is shown in Figure 1, and described as a programming voltage at page 3, lines 5-7.

DUPLICATE

Claims 1-3, 5-13, 20 and 21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 has been amended to replace the misdescriptive term "a switched capacitor circuit" with a reference to a "ramp generator." The ramp generator is shown as block 11 in Figure 1, and comprises a first capacitor and a second capacitor.

Claim 6 has been canceled.

Claim 7 has been amended to delete the phrase "to shut off said signal."

Claim 11 has been amended to delete the reference to "a constant reference voltage according to a feedback system." Claim 11 has also been amended to depend from Claim 10

Claim 20 has been amended to refer to clarify programming voltage by referencing the program voltage to VPP. The power supply voltage has also been referenced to VCC. Then generation of VPP from VCC is described on page 3, lines 5-7, and elsewhere in the specification

In summary, Applicant asserts that Claims 1-3, 5, 7-13, and 20-21 are in condition for allowance and earnestly solicits such action by the Examiner.

Please charge any additional fees or apply any credits to our PTO deposit account number: 23-0085.

DUPLICATE

Respectfully submitted,

WAGNER, MURABITO & HAO

Date: August 6, 2003

Mehlin Dean Matthews
Registration Number: 46,127

WAGNER, MURABITO & HAO
Two North Market Street
Third Floor
San Jose, CA 95113

408-938-9060

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Replacement Sheet

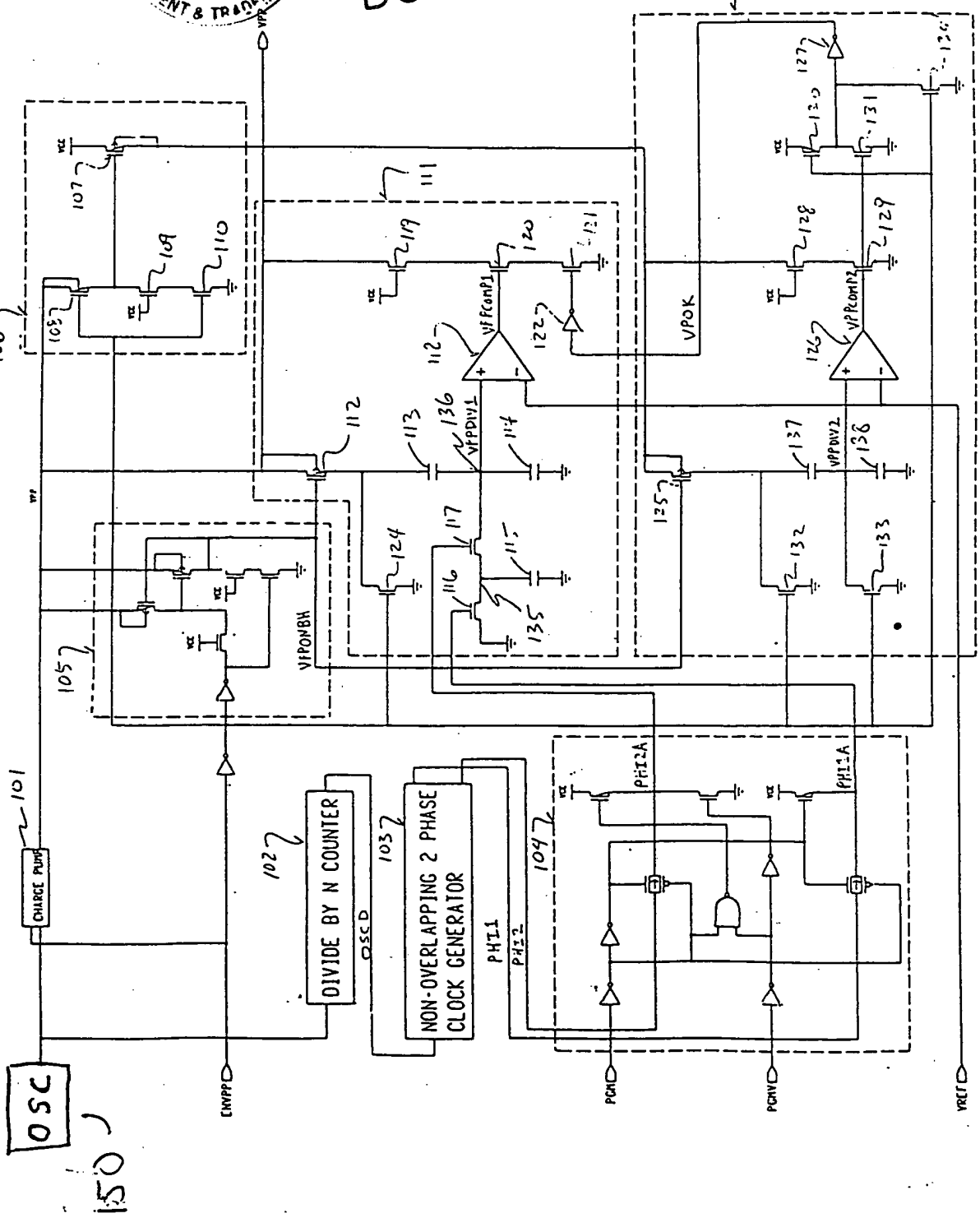

Figure 1

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